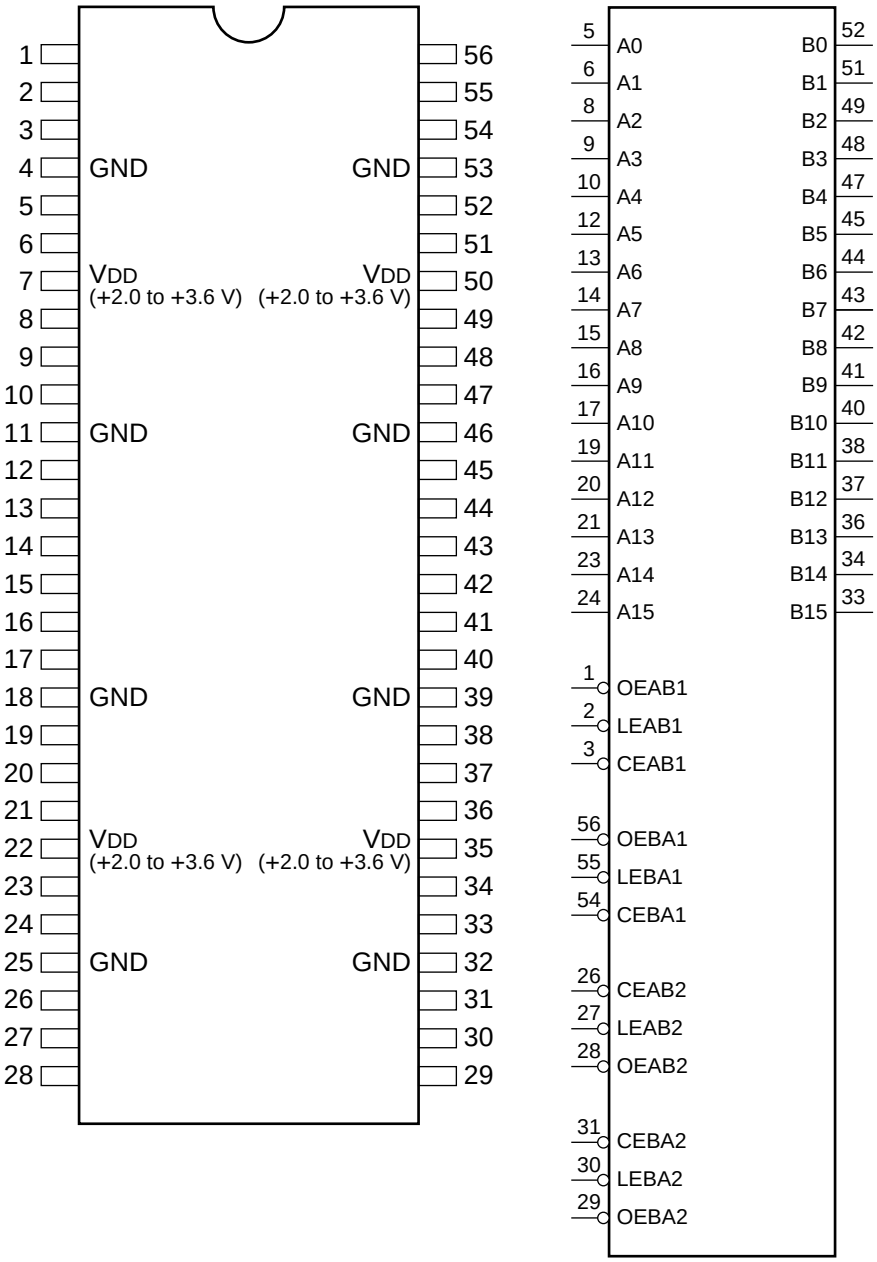
C-MOS 16-BIT REGISTERED TRANSCEIVER

—TOP VIEW—



(V_{DD} = +2.0 to +3.6 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{OEAB1}$	15	I/O	A8	29	I	$\overline{OEBA2}$	43	I/O	B7
2	I	$\overline{LEAB1}$	16	I/O	A9	30	I	$\overline{LEBA2}$	44	I/O	B6
3	I	$\overline{CEAB1}$	17	I/O	A10	31	I	$\overline{CEBA2}$	45	I/O	B5
4	—	GND	18	—	GND	32	—	GND	46	—	GND
5	I/O	A0	19	I/O	A11	33	I/O	B15	47	I/O	B4
6	I/O	A1	20	I/O	A12	34	I/O	B14	48	I/O	B3
7	—	V_{DD}	21	I/O	A13	35	—	V_{DD}	49	I/O	B2
8	I/O	A2	22	—	V_{DD}	36	I/O	B13	50	—	V_{DD}
9	I/O	A3	23	I/O	A14	37	I/O	B12	51	I/O	B1
10	I/O	A4	24	I/O	A15	38	I/O	B11	52	I/O	B0
11	—	GND	25	—	GND	39	—	GND	53	—	GND
12	I/O	A5	26	I	$\overline{CEAB2}$	40	I/O	B10	54	I	$\overline{CEBA1}$
13	I/O	A6	27	I	$\overline{LEAB2}$	41	I/O	B9	55	I	$\overline{LEBA1}$
14	I/O	A7	28	I	$\overline{OEAB2}$	42	I/O	B8	56	I	$\overline{OEBA1}$

INPUT

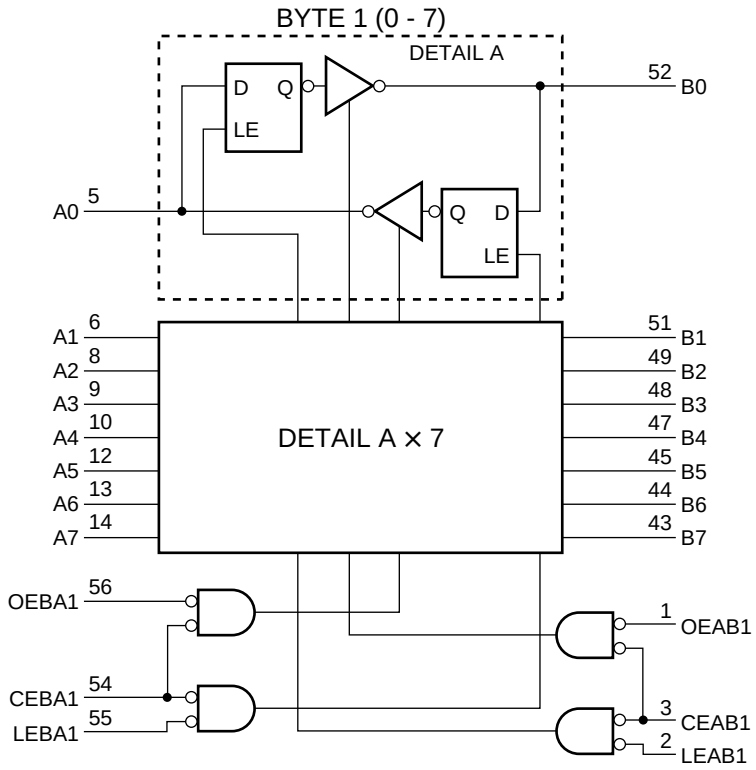
CEAB : A-TO-B ENABLE
CEBA : B-TO-A ENABLE
LEAB : A-TO-B LATCH ENABLE
LEBA : B-TO-A LATCH ENABLE
OEAB : A-TO-B OUTPUT ENABLE
OEBA : B-TO-A OUTPUT ENABLE

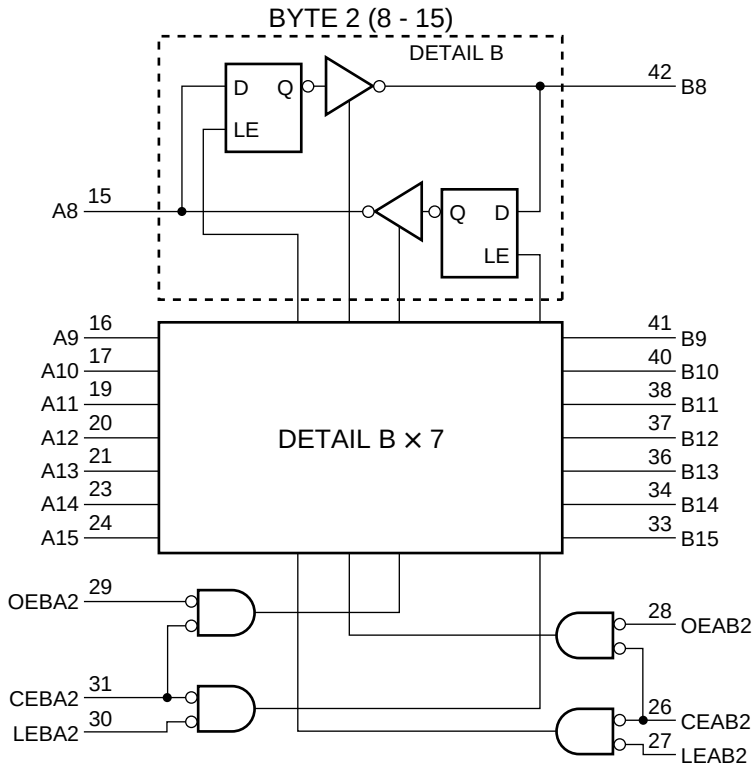
INPUT/OUTPUT

A0 - A15 : A-TO-B DATA INPUTS OR B-TO-A TRI-STATE OUTPUTS
B0 - B15 : B-TO-A DATA INPUTS OR A-TO-B TRI-STATE OUTPUTS

INPUTS			LATCH STATUS (BYTE n)	OUTPUT BUFFERS (BYTE n)
$\overline{CEABn}$	$\overline{LEABn}$	$\overline{OEABn}$		
1	×	×	LATCHED	HI-Z
×	1	×	LATCHED	—
0	0	×	TRANSPARENT	—
×	×	1	—	HI-Z
0	×	0	—	DRIVING

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE


BYTE 1 (0 - 7)
DETAIL A
D
Q
LE
Q
D
LE
A0
5
52
B0
A1
6
A2
8
A3
9
A4
10
A5
12
A6
13
A7
14
DETAIL A × 7
51
B1
49
B2
48
B3
47
B4
45
B5
44
B6
43
B7
OEBA1
56
CEBA1
54
LEBA1
55
1
OEAB1
3
CEAB1
2
LEAB1


BYTE 2 (8 - 15)
DETAIL B
D
Q
LE
Q
D
LE
A8
15
42
B8
A9
16
A10
17
A11
19
A12
20
A13
21
A14
23
A15
24
DETAIL B × 7
41
B9
40
B10
38
B11
37
B12
36
B13
34
B14
33
B15
OEBA2
29
CEBA2
31
LEBA2
30
28
OEAB2
26
CEAB2
27
LEAB2